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10/816,413	03/31/2004	Chi Shen Ho	68,700-017	8846

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,413	HO, CHI SHEN	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-26,28-36,38 and 40-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-26,28-36,38 and 40-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 42-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 42-44 are recites the limitation the substrate in claims 42-44. There is insufficient antecedent basis for this limitation in the claim. If the Applicant is trying to claim the semiconductor carrier substrate then there will be a duplicate claim double patenting rejection placed on these claims because claims 7, 15, and 35 already claim these limitations.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 11, 14, 16, 18-22, 25, 28, 30, 32-36, 38, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,087,991 Chen et al. in view of U.S. Patent No. 6,825,553 Chua et al. in further view of U.S. Patent No. 7,074,650 Honda.

1. Referring to claim 1, a method of making a semiconductor package comprising: providing a semiconductor chip carrier substrate, (Chen et al. Figure 3A-I #310), having a first surface and a plurality of cavities, (Chen et al. Figure 3A-I area of #314 and Chau et al. Figure 2

#205 and See * below), formed in the first surface and wherein each cavity, (Chen et al. Figure 3A-I area of #314 and Chau et al. Figure 2 #205 and See * below), is defined, at least in part, by a bottom surface and at least one sidewall; placing an integrated circuit chip, (Chen et al. Figures 3A-I #400), having bond pads, (Chen et al. Figures 3A-I #406), on an upper surface thereof, in each of the cavities, (Chen et al. Figure 3A-I area of #314 and Chau et al. Figure 2 #205 and See * below), formed in the chip carrier substrate, (Chen et al. Figures 3A-I #310), and wherein each semiconductor chip, (Chen et al. Figures 3A-I #400), overlies the bottom surface; and forming a first dielectric layer, (Chen et al. Figures 3A-I #320), over the first surface of the chip carrier substrate, (Chen et al. Figures 3A-I #310), and over the integrated circuit chip, (Chen et al. Figures 3A-I #400), in each of the cavities, (Chen et al. Figure 3A-I area of #314 and Chau et al. Figure 2 #205 and See * below), wherein the first dielectric layer comprises at least one of a polyimide and BCB, (Chen et al. Figures 3A-I #320 and See ** below).

* Chen et al. discloses the claimed invention except for the specific illustration of multiple cavities, but does teach that there is at least one in Col. 2 Lines 50-51. Chau et al. teaches of a very similar device with multiple cavities with multiple ICs in each of the cavities in Figure 2. It would have been obvious to one having skill in the art at the time the invention was made to make multiple cavities with an IC in each of the cavites and where the process of dicing would separate into individual packages, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art and where forming a wafer and later dicing reduces the cost and time for producing multiple packages. St. Regis Paper Co. vs. Bomis Co. 193USPQ8

** Chen et al. is silent to the specific material used for the first and second dielectric layers. Chua et al. also is silent on the exact material used for the first and second dielectric layers in Figure 2, but teaches the dielectric material used in the first embodiment to be a polyimide in Col. 5 Lines 61-62. Honda teaches of a very similar device with conductive traces leading to the outside of the package and where the dielectric material used between the traces and the conductive bumps to be of a polyimide and BCB material, (#4 Col. 7 Lines 21-22 and #20 Col. 11 Line 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first and second dielectric layers out of a polyimide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

2. Referring to claim 2, a method as set forth in Claim 1 further comprising forming a first set of vias, (Chen et al. Figures 3A-I #322), in the first dielectric layer, (Chen et al. Figures 3A-I #310), and so that each of the first set of vias, (Chen et al. Figures 3A-I #322), is aligned with a respective bond pad, (Chen et al. Figures 3A-I #406), of the integrated circuit chip, (Chen et al. Figures 3A-I #400).

3. Referring to claim 3, a method as set forth in Claim 2 further comprising forming an electrically conductive traces, (Chen et al. Figures 3A-I #340), over the first dielectric layer, (Chen et al. Figures 3A-I #320), and so that each one of the electrically conductive traces, (Chen et al. Figures 3A-I #340), are electrically connected to at least one of the bond pads, (Chen et al. Figures 3A-I #406), of the integrated circuit chip, (Chen et al. Figures 3A-I #400).

4. Referring to claim 4, a method as set forth in Claim 3 further comprising forming a second dielectric layer, (Chen et al. Figures 3A-I #320), over the redistribution traces, (Chen et al. Figures 3A-I #340), and forming a second set of vias, (Chen et al. Figures 3A-I #346), in the second dielectric layer, (Chen et al. Figures 3A-I #320), so that each of the second set of vias, (Chen et al. Figures 3A-I #346), communicates with one of the redistribution traces, (Chen et al. Figures 3A-I #340).

5. Referring to claim 5, a method as set forth in Claim 4 further comprising forming electrically conductive bumps, (Chen et al. Figures 3A-I #360), wherein each electrically conductive bump, (Chen et al. Figures 3A-I #360), overlies the second dielectric layer, (Chen et al. Figures 3A-I #320), and comprises an unrounded portion extending into one of the vias, (Chen et al. Figures 3A-I #346), formed in the second dielectric layer, (Chen et al. Figures 3A-I #320), and so that the electrically conductive bump, (Chen et al. Figures 3A-I #360), is electrically connected to one of the redistribution traces, (Chen et al. Figures 3A-I #340).

6. Referring to claim 6, a method as set forth in Claim 5 further comprising sectioning the semiconductor chip carrier into individual packages each including a semiconductor chip, (See * above).

7. Referring to claim 7, a method as set forth in Claim 1 wherein the semiconductor chip carrier comprises at least one of silicone, glass, ceramic, and plastic, (Chen et al. Col. 5 Lines 38-39).

8. Referring to claim 8, a method as set forth in Claim 1 wherein the plurality of cavities are formed by etching a semiconductor chip carrier substrate, (Chen et al. 3 Lines 50-51 and Chau et al. Col. 3 Lines 61-63).

9. Referring to claim 11, a method as set forth in Claim 1 further comprising depositing an adhesive, (Chen et al. Figures 3A-I #410), over the bottom surface defining each cavity, (Chen et al. Figures 3A-I #314), prior to placing the integrated circuit chip, (Chen et al. Figures 3A-I #400), in each cavity.

10. Referring to claim 14, a method as set forth in Claim 3 wherein the electrically conductive redistribution traces comprise copper, (Chen et al. Figures 3A-I #340 and Chau et al. Col. 8 Lines 2-4).

*** Chen et al. discloses the claimed invention except for the traces being made out of Cu, but Chau et al. does in Col. 8 Lines 2-4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the traces out of Copper, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.
In re Leshin, 125 USPQ 416.

11. Referring to claim 16, a method as set forth in Claim 4 wherein the second dielectric layer comprises at least one of a polyimide and BCB, (See ** above).

12. Referring to claim 18, a method as set forth in Claim 5 wherein the electrically conductive bumps are formed by at least one of ball placement, (Chen et al. Figures 3A-I #360 Col. 4 Lines 52-54), stenciling, and plating.

13. Referring to claim 19, a method as set forth in Claim 6 wherein the sectioning comprises cutting the chip carrier substrate with a saw, (Chau et al. Col. 8 Line 48 and See * above).

14. Referring to claim 20, a method of making a semiconductor package comprising: providing a wafer size semiconductor chip carrier substrate, (Chen et al. Figures 3A-I #400),

having a first surface and a plurality of cavities, (Chen et al. Figures 3A-I #314 and See * below), formed in the first surface and wherein each cavity, (Chen et al. Figures 3A-I #314 abd See * below), is defined, at least in part, by a bottom surface and at least one sidewall; placing an integrated circuit chip, (Chen et al. Figures 3A-I #400), having bond pads, (Chen et al. Figures 3A-I #406), on an upper surface thereof, in each of the cavities, (Chen et al. Figures 3A-I #314), formed in the wafer size chip carrier substrate, (Chen et al. Figures 3A-I #310), and wherein each semiconductor chip, (Chen et al. Figures 3A-I #400), overlies the bottom surface; forming a first dielectric layer, (Chen et al. Figures 3A-I #320), over the first surface of the chip carrier substrate, (Chen et al. Figures 3A-I #310), and over the integrated circuit chip, (Chen et al. Figures 3A-I #400), in each of the cavities, (Chen et al. Figures 3A-I #314); wherein the first dielectric layer comprises at least one of a polyimide and BCB, (Chen et al. Figures 3A-I #320 and See ** below); forming a first set of vias, (Chen et al. Figures 3A-I #322), in the first dielectric layer, (Chen et al. Figures 3A-I #320), and so that each of the first set of vias, (Chen et al. Figures 3A-I #322), is aligned with a respective bond pad, (Chen et al. Figures 3A-I #406), of the integrated circuit chip, (Chen et al. Figures 3A-I #400); forming an electrically conductive layer over, (Chen et al. Figures 3A-I #340), the first dielectric layer, (Chen et al. Figures 3A-I #320), and down into the vias, (Chen et al. Figures 3A-I #322), formed in the first dielectric layer, (Chen et al. Figures 3A-I #320), and selectively removing portions, (Chen et al. Figures 3E-G), of the electrically conductive layer, (Chen et al. Figures 3A-I #340), to form electrically conductive traces, (Chen et al. Figures 3A-I #340), and so that each one of the electrically conductive traces, (Chen et al. Figures 3A-I #340), is electrically connected to at least one of the bond pads, (Chen et al. Figures 3A-I #406), of the integrated circuit chip, (Chen et al. Figures

3A-I #400); forming a second dielectric, (Chen et al. Figures 3A-I #320), over the redistribution traces, (Chen et al. Figures 3A-I #340), and forming a second set of vias, (Chen et al. Figures 3A-I #346), in the second dielectric layer, (Chen et al. Figures 3A-I #320), so that each of the second set of vias communicates, (Chen et al. Figures 3A-I #346), with one of the redistribution traces, (Chen et al. Figures 3A-I #340); forming electrically conductive bumps, (Chen et al. Figures 3A-I #360), wherein each electrically conductive bump, (Chen et al. Figures 3A-I #360), overlies the second dielectric layer, (Chen et al. Figures 3A-I #320), and comprises an unrounded portion extending into one of the vias, (Chen et al. Figures 3A-I #346), formed in the second dielectric layer, (Chen et al. Figures 3A-I #320), and so that the electrically conductive bump, (Chen et al. Figures 3A-I #360), is electrically connected to one of the redistribution traces, (Chen et al. Figures 3A-I #340); and sectioning the semiconductor chip carrier, (Chen et al. Figures 3A-I #310), so into individual packages each including a semiconductor chip, (See * below).

* Chen et al. discloses the claimed invention except for the specific illustration of multiple cavities, but does teach that there is at least one in Col. 2 Lines 50-51. Chau et al. teaches of a very similar device with multiple cavities with multiple ICs in each of the cavities in Figure 2. It would have been obvious to one having skill in the art at the time the invention was made to make multiple cavities with an IC in each of the cavites and where the process of dicing would separate into individual packages, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art and where forming a wafer and later dicing reduces the cost and time for producing multiple packages. St. Regis Paper Co. vs. Bomis Co. 193USPQ8

** Chen et al. is silent to the specific material used for the first and second dielectric layers. Chua et al. also is silent on the exact material used for the first and second dielectric layers in Figure 2, but teaches the dielectric material used in the first embodiment to be a polyimide in Col. 5 Lines 61-62. Honda teaches of a very similar device with conductive traces leading to the outside of the package and where the dielectric material used between the traces and the conductive bumps to be of a polyimide and BCB material, (#4 Col. 7 Lines 21-22 and #20 Col. 11 Line 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first and second dielectric layers out of a polyimide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

15. Referring to claim 21, a method as set forth in Claim 20 wherein the semiconductor chip carrier, (Chen et al. Figures 3A-I #310), comprises at least one of silicone, glass, ceramic, and plastic, (Chen et al. Col. 5 Lines 38-39).

16. Referring to claim 22, a method as set forth in Claim 20 wherein the plurality of cavities are formed by etching a semiconductor chip carrier substrate, (Chen et al. 3 Lines 50-51 and Chau et al. Col. 3 Lines 61-63).

17. Referring to claim 25, a method as set forth in Claim 20 further comprising depositing an adhesive, (Chen et al. Figures 3A-I #410), over the bottom surface defining each cavity, (Chen et al. Figures 3A-I #314), prior to placing the integrated circuit chip, (Chen et al. Figures 3A-I #400), in each cavity.

18. Referring to claim 28, a method as set forth in Claim 20 wherein the electrically conductive redistribution traces comprise copper, (Chen et al. Figures 3A-I #340 and Chau et al. Col. 8 Lines 2-4).

*** Chen et al. discloses the claimed invention except for the traces being made out of Cu, but Chau et al. does in Col. 8 Lines 2-4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the traces out of Copper, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

In re Leshin, 125 USPQ 416.

19. Referring to claim 30, a method as set forth in Claim 20 wherein the second dielectric layer comprises at least one of a polyimide and BCB, (See ** above).

20. Referring to claim 32, a method as set forth in Claim 20 wherein the electrically conductive bumps are formed by at least one of ball placement, (Chen et al. Figures 3A-I #360 Col. 4 Lines 52-54), stenciling, and plating.

21. Referring to claim 33, a method as set forth in Claim 20 wherein the sectioning comprises cutting the chip carrier substrate with a saw, (Chau et al. Col. 8 Line 48 and See * above).

22. Referring to claim 34, a semiconductor package comprising: a semiconductor chip carrier substrate, (Chen et al. Figures 3A-I #310), having a first surface and a plurality of cavities, (Chen et al. Figures 3A-I #314 and See * below), formed in the first surface and wherein each cavity, (Chen et al. Figures 3A-I #314), is defined, at least in part, by a bottom surface and at least one sidewall; an integrated circuit chip, (Chen et al. Figures 3A-I #400), having bond pads, (Chen et al. Figures 3A-I #406), on an upper surface thereof, in each of the cavities, (Chen et al. Figures

3A-I #314), formed in the chip carrier substrate, (Chen et al. Figures 3A-I #310), and wherein each semiconductor chip, (Chen et al. Figures 3A-I #400), overlies the bottom surface; a first dielectric layer, (Chen et al. Figures 3A-I #320), over the first surface of the chip carrier substrate, (Chen et al. Figures 3A-I #310), and over the integrated circuit chip, (Chen et al. Figures 3A-I #400), in each of the cavities, (Chen et al. Figures 3A-I #314); wherein the first dielectric layer comprises at least one of a polyimide and BCB, (Chen et al. Figures 3A-I #320 and See ** below); a first set of vias, (Chen et al. Figures 3A-I #322), in the first dielectric layer, (Chen et al. Figures 3A-I #320), and so that each vias is aligned with a respective bond pad, (Chen et al. Figures 3A-I #406), of the integrated circuit chip, (Chen et al. Figures 3A-I #400); electrically conductive traces, (Chen et al. Figures 3A-I #340), over the first dielectric layer, (Chen et al. Figures 3A-I #320), and one of the traces, (Chen et al. Figures 3A-I #340), extending down into one of the vias, (Chen et al. Figures 3A-I #406), formed in the first dielectric layer, (Chen et al. Figures 3A-I #320), so that each one of the electrically conductive traces, (Chen et al. Figures 3A-I #340), is electrically connected to at least one of the bond pads, (Chen et al. Figures 3A-I #406), of the integrated circuit chip, (Chen et al. Figures 3A-I #400); a second dielectric layer, (Chen et al. Figures 3A-I #320), over the redistribution traces, (Chen et al. Figures 3A-I #340), and a second set of vias, (Chen et al. Figures 3A-I #346), in the second dielectric layer, (Chen et al. Figures 3A-I #320), so that each of the second set of vias communicates, (Chen et al. Figures 3A-I #346), with one of the redistribution traces, (Chen et al. Figures 3A-I #340); electrically conductive bumps, (Chen et al. Figures 3A-I #360), wherein each electrically conductive bump, (Chen et al. Figures 3A-I #360), overlies the second dielectric layer, (Chen et al. Figures 3A-I #320), and comprises an unrounded portion extending into one of

the vias, (Chen et al. Figures 3A-I #346), formed in the second dielectric layer, (Chen et al. Figures 3A-I #320), and so that the electrically conductive bump, (Chen et al. Figures 3A-I #360), is electrically connected to one of the redistribution traces, (Chen et al. Figures 3A-I #340).

* Chen et al. discloses the claimed invention except for the specific illustration of multiple cavities, but does teach that there is at least one in Col. 2 Lines 50-51. Chau et al. teaches of a very similar device with multiple cavities with multiple ICs in each of the cavities in Figure 2. It would have been obvious to one having skill in the art at the time the invention was made to make multiple cavities with an IC in each of the cavites and where the process of dicing would separate into individual packages, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art and where forming a wafer and later dicing reduces the cost and time for producing multiple packages. St. Regis Paper Co. vs. Bomis Co. 193USPQ8

** Chen et al. is silent to the specific material used for the first and second dielectric layers. Chua et al. also is silent on the exact material used for the first and second dielectric layers in Figure 2, but teaches the dielectric material used in the first embodiment to be a polyimide in Col. 5 Lines 61-62. Honda teaches of a very similar device with conductive traces leading to the outside of the package and where the dielectric material used between the traces and the conductive bumps to be of a polyimide and BCB material, (#4 Col. 7 Lines 21-22 and #20 Col. 11 Line 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first and second dielectric layers out of a polyimide, since it has been held to be within the general skill of a worker in the art to select a known material on the

basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

23. Referring to claim 35, a semiconductor package as set forth in Claim 34 wherein the semiconductor chip carrier, (Chen et al. Figures 3A-I #310), comprises at least one of silicone, glass, ceramic, and plastic, (Chen et al. Col. 5 Lines 38-39).

24. Referring to claim 36, a semiconductor package as set forth in Claim 34 further comprising an adhesive, (Chen et al. Figures 3A-I #410), over the bottom surface defining each cavity, (Chen et al. Figures 3A-I #314), prior to placing the integrated circuit chip, (Chen et al. Figures 3A-I #400), in each cavity.

25. Referring to claim 38, a semiconductor package as set forth in Claim 34 wherein the electrically conductive redistribution traces comprise copper, (Chen et al. Figures 3A-I #340 and Chau et al. Col. 8 Lines 2-4).

*** Chen et al. discloses the claimed invention except for the traces being made out of Cu, but Chau et al. does in Col. 8 Lines 2-4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the traces out of Copper, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.
In re Leshin, 125 USPQ 416.

26. Referring to claim 41, a semiconductor package as set forth in Claim 34 wherein the second dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62 and See ** above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15, 29, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,087,991 Chen et al. in view of U.S. Patent No. 6,825,553 Chua et al. in further view of U.S. Patent No. 7,074,650 Honda. in further view of U.S. Patent No. 6,617,674 Becker et al.

27. Referring to claim 15, a method as set forth in Claim 14 wherein the electrically conductive redistribution traces further comprise nickel, (Becker et al. Col. 9 Lines 25-28 and See *** below).

*** Chen et al, Chua et al., and Honda discloses the claimed invention except for the traces being also made with nickel, but Becker et al. does in Col. 9 Lines 25-28. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Chua et al. with the teachings of Becker et al. because adding nickel to the copper traces provides a diffusion barrier to the traces, (Becker et al. col. 9 Lines 25-28), and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.
In re Leshin, 125 USPQ 416.

28. Referring to claim 29, a method as set forth in Claim 28 wherein the electrically conductive redistribution traces further comprise nickel, (Becker et al. Col. 9 Lines 25-28 and See *** above).

29. Referring to claim 40, a semiconductor package as set forth in Claim 38 wherein the electrically conductive redistribution traces further comprise nickel, (Becker et al. Col. 9 Lines 25-28 and See *** above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,087,991 Chen et al. in view of U.S. Patent No. 6,825,553 Chua et al. in further view of U.S. Patent No. 7,074,650 Honda. in further view of U.S. Patent No. 6,548,895 Benavides et al.

30. Referring to claim 9, a method as set forth in Claim 1 wherein the cavities are formed by molding the semiconductor circuit chip carrier substrate to provide the cavities, (Benavides et al. Col. 10 Lines 33-35 and See **/* below).

**/* Chen et al, Chua et al., and Honda teaches all of the claimed matter in claims 9, 10, 23, & 24, but is silent on the process of forming the cavity in a carrier by molding or milling, but Benavides et al. does in Col. 10 Lines 33-35. It would have been obvious to one having skill in the art at the time the invention was made to make a cavity by a mold process or by a milling

process. These processes are known equivalents to an etching process as taught by Chua et al. in Col. 3 Lines 61-63, and where this alternative lacks an inventive step.

31. Referring to claim 10, a method as set forth in Claim 1 wherein the cavities are provided by milling a flat surface of a semiconductor chip carrier substrate, (Benavides et al. Col. 10 Lines 33-35 and See **/* above).

32. Referring to claim 23, a method as set forth in Claim 20 wherein the cavities are formed by molding the semiconductor circuit chip carrier substrate to provide the cavities, (Benavides et al. Col. 10 Lines 33-35 and See **/* above).

33. Referring to claim 24, a method as set forth in Claim 20 wherein the cavities are provided by milling a flat surface of a semiconductor chip carrier substrate, (Benavides et al. Col. 10 Lines 33-35 and See **/* above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,087,991 Chen et al. in view of U.S. Patent No. 6,825,553 Chua et al. in further view of U.S. Patent No. 7,074,650 Honda. in further view of U.S. Patent No. 5,106,461 Volfson et al.

34. Referring to claim 12, a method as set forth in Claim 2 wherein the first set of vias formed in the first dielectric layer are formed by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** below).

**** Chen et al, Chua et al., and Honda teaches all of the claimed matter in claims 12, 17, 26, and 31 but is silent in the respect of teaching the narrowed process of ion etching being used to form a via. Chen et al. teaches the etching process in Figure 3 3F-3G and Chua et al. teaches etching the dielectric layer to form a via in Col. 8 Lines 15-16. Volfson et al. does teach the process of forming a via by the narrowed technique of ion etching in Col. 8 Lines 4-8. It would have been obvious tone having skill in the art to use the narrowed ion etching process to form a via and where these processes are known equivalents, and where this alternative lacks an inventive step.

35. Referring to claim 17, a method as set forth in Claim 4 wherein the second set of vias is formed in the second dielectric layer by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** above).

36. Referring to claim 26, a method as set forth in Claim 21 wherein the first set of vias formed in the first dielectric layer are formed by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** above).

37. Referring to claim 31, a method as set forth in Claim 20 wherein the second set of vias is formed in the second dielectric layer by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** above).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
9/4/06

EVAN PERT
PRIMARY EXAMINER